## CLAIM AMENDMENTS

Please amend the claims as described below. In accordance with 37 CFR §1.121, a complete listing of all claims in the application is provided below. Notably, the status of each claim is indicated in the parenthetical expression adjacent to the claim number.

Claims 1 - 27 (**canceled**).

28. (**Currently Amended**): A semiconductor memory array comprising:

a plurality of memory cells arranged in a matrix of rows and columns, the plurality of memory cells ~~include~~ includes a first memory cell and a second memory cell, wherein the first and second memory cells each ~~include~~ includes at least a transistor to constitute the memory cell and wherein the transistor includes:

a source region;

a drain region;

a body region disposed between and adjacent to the source region and the drain region, wherein the body region is an electrically floating state; and

a gate disposed over the body region;

wherein each memory cell includes:

a first data state representative of a first charge in the body region; and

a second data state representative of a second charge in the body region wherein the second charge is substantially provided by removing charge from the body region through the source region; and

wherein the gate of the transistor of the first memory cell and the gate of the transistor of the second memory cell are connected.

29. (**Currently Amended**): The memory array of claim 28 wherein:

the plurality of memory cells further includes a third memory cell and a fourth memory cell, wherein the third and fourth memory cells each ~~include~~ includes at least a transistor to constitute the memory cell and wherein the transistor includes:

a source region;

a drain region;

a body region disposed between and adjacent to the source region and the drain region, wherein the body region is an electrically floating state; and

a gate disposed over the body region;

wherein each memory cell includes:

a first data state representative of a first charge in the body region; and

a second data state representative of a second charge in the body region wherein the second charge is substantially provided by removing charge from the body region through the source region; and

wherein the source region of the transistor of the first memory cell and the source region of the transistor of the third memory cell are the same region and wherein the drain region of the transistor of the first memory cell and the drain region of the transistor of the fourth memory cell are the same region.

30. (**Currently Amended**): The memory array of claim 28 wherein the first charge is comprised of an accumulation of majority carriers in the body region of the transistor of the first memory cell.

31. (**Currently Amended**): The memory array of claim 30 wherein the majority carriers accumulate in a portion of the body region ~~regions~~ that is adjacent to the source region ~~regions~~ of the transistor of each memory cell of the plurality of memory cells.

32. (**Currently Amended**): The memory array of claim 28 further including a control unit, coupled to the gate and the drain region of the first memory cell, to provide control signals to the first ~~and second~~ memory cell ~~cells~~, wherein the first memory cell, in response to ~~a~~ first write control signals ~~signal set~~, stores the first charge in the body region of the transistor of the first memory cell.

33. (**Currently Amended**): The memory array of claim 28 ~~32~~ further including a control unit, coupled to the gate and the drain region of the first memory cell, to provide control signals to the first ~~and second~~ memory cell ~~cells~~, wherein the first memory cell, in response to ~~a~~ second write control signals ~~signal set~~, stores the second charge in the body region of the transistor of the first memory cell by removing charge from the body region of the transistor of the first memory cell through its source region.

34. (**Currently Amended**): The memory array of claim 33 wherein the control unit applies positive voltages to the drain region and gate of the transistor of the first memory cell to provide the second charge in the body region of the transistor of the first memory cell.

35. (**Currently Amended**): The memory array of claim 34 wherein the control unit is coupled to the gate, drain region and source region of the transistor of the second memory cell and applies positive voltages to the drain region and gate of the transistor of the first memory cell to provide the second charge in the body region of the transistor of the first memory cell and applies a first voltage to the drain and source regions of the transistor of the second memory cell to maintain the data state of the second memory cell.

36. (**Previously Presented**): The memory array of claim 35 wherein the first voltage is ground.

37. (**Currently Amended**): A semiconductor memory array comprising:

a plurality of memory cells arranged in a matrix of rows and columns, the plurality of memory cell ~~include~~ includes a first memory cell and a second memory cell, wherein the first and second memory cells each ~~include~~ includes at least a transistor to constitute the memory cell and wherein the transistor includes:

a source region having impurities to provide a first conductivity type;

a drain region having impurities to provide the first conductivity type,

a body region disposed between and adjacent to the source region and the drain region wherein the body region is electrically floating and includes impurities to provide a second conductivity type wherein the second conductivity type is different than the first conductivity type;

a gate disposed over the body region;

wherein the memory cell includes:

a first data state representative of a first charge in the body region wherein the first charge is substantially provided by impact ionization; and

a second data state representative of a second charge in the body region wherein the second charge is substantially provided by removing charge from the body region through the source region; and

wherein the gate of the transistor of the first memory cell and the gate of the transistor of the second memory cell are connected.

38. (**Currently Amended**): The memory array of claim 37 wherein:

the plurality of memory cells further includes a third memory cell wherein the third memory cell includes at least a transistor to constitute the memory cell wherein the transistor includes:

a source region having impurities to provide ~~a~~ the first conductivity type;

a drain region having impurities to provide the first conductivity type,

a body region disposed between and adjacent to the source region and the drain region wherein the body region is electrically floating and includes impurities to provide ~~a~~ the second conductivity type wherein the second conductivity type is different than the first conductivity type;

a gate disposed over the body region; and

wherein the memory cell includes:

a first data state representative of a first charge in the body region wherein the first charge is substantially provided by impact ionization; and

a second data state representative of a second charge in the body region wherein the second charge is substantially provided by removing charge from the body region through the source region; and

wherein the source region of the transistor of the first memory cell and the source region of the transistor of the third memory cell are the same region.

39. (**Currently Amended**): The memory array of claim 37 wherein:

the plurality of memory cells further includes a fourth memory cell wherein the fourth memory cell includes at least a transistor to constitute the memory cell wherein the transistor includes:

a source region having impurities to provide ~~a~~ the first conductivity type;

a drain region having impurities to provide the first conductivity type,

a body region disposed between and adjacent to the source region and the drain region wherein the body region is electrically floating and includes impurities to provide ~~a~~ the second conductivity type wherein the second conductivity type is different than the first conductivity type;

a gate disposed over the body region,

wherein the memory cell includes:

a first data state representative of a first charge in the body region wherein the first charge is substantially provided by impact ionization; and

a second data state representative of a second charge in the body region wherein the second charge is substantially provided by removing charge from the body region through the source region; and

wherein the drain region of the transistor of the first memory cell and the drain region of the transistor of the fourth memory cell are the same region.

40. (**Currently Amended**): The memory array of claim 39 wherein the first charge is comprised of an accumulation of majority carriers in the body region of the transistor of the first memory cell.

41. (**Currently Amended**): The memory array of claim 40 wherein the majority carriers accumulate in a portion of the body region ~~regions~~ that is adjacent to the source region ~~regions~~ of the transistor of each memory cell of the plurality of memory cells.

42. (**Currently Amended**): The memory array of claim 39 further including a control unit, coupled to the gate and the drain region of the transistor of the first memory cell, to provide control signals to the first ~~and second~~ memory cell ~~cells~~, wherein the first memory cell, in response to ~~a~~ first write control signals ~~signal set~~, stores the first charge in the body region of the transistor of the first memory cell.

43. (**Currently Amended**): The memory array of claim 39 ~~42~~ further including a control unit, coupled to the gate and the drain region of the transistor of the first memory cell, to provide control signals to the first ~~and second~~ memory cell ~~cells~~, wherein the first memory cell, in response to ~~a~~ second write control signals ~~signal set~~, stores the second charge in the body region of the transistor of the first memory cell by removing charge from the body region of the transistor of the first memory cell through its source region.

44. (**Currently Amended**): The memory array of claim 43 wherein the control unit applies positive voltages to the drain region and gate of the transistor of the first memory cell to provide the second charge in the body region of the transistor of the first memory cell.

45. (**Currently Amended**): The memory array of claim 44 wherein the control unit is coupled to the gate, drain region and source region of the transistor of the second memory cell and applies positive voltages to the drain region and gate of the transistor of the first memory cell to provide the second charge in the body region of the transistor of the first memory cell and applies a first voltage to the drain and source regions of the transistor of the second memory cell to maintain the data state of the second memory cell.

46. (**Previously Presented**): The memory array of claim 45 wherein the first voltage is ground.

47. (**Currently Amended**): A semiconductor memory array, disposed in or on a semiconductor layer which resides on or above an insulating layer of a substrate, the semiconductor memory array comprising:

a plurality of memory cells, including a first memory cell and a second memory cell, arranged in a matrix of rows and columns and disposed in or on the semiconductor layer, ~~including a first memory cell and a second memory cell,~~ wherein the first and second memory cells each ~~include~~ includes at least a transistor to constitute the memory cell and wherein the transistor includes:

a source region having impurities to provide a first conductivity type;

a drain region having impurities to provide the first conductivity type,

a body region disposed between and adjacent to the source region, ~~and~~ the drain region and the insulating layer of the substrate, wherein the body region is electrically floating and includes impurities to provide a second conductivity type wherein the second conductivity type is different than the first conductivity type;

a gate spaced apart from, and capacitively coupled to, the body region;

wherein the memory cell includes:

a first data state representative of a first charge in the body; and

a second data state representative of a second charge in the body region wherein the second charge is substantially provided by removing charge from the body region through the source region; and

wherein the gate of the transistor of the first memory cell and the gate of the transistor of the second memory cell are connected.

48. (**Currently Amended**): The memory array of claim 47 wherein:

the plurality of memory cells further includes a third memory cell wherein the third memory cell includes at least a transistor to constitute the memory cell wherein the transistor includes:

a source region having impurities to provide the ~~a~~ first conductivity type;

a drain region having impurities to provide the first conductivity type;

a body region disposed between and adjacent to the source region and the drain region wherein the body region is electrically floating and includes

impurities to provide the ~~a~~ second conductivity type wherein the second conductivity type is different than the first conductivity type;

a gate spaced apart from, and capacitively coupled to, the body region; and

wherein the memory cell includes:

a first data state representative of a first charge in the body; and

a second data state representative of a second charge in the body region wherein the second charge is substantially provided by removing charge from the body region through the source region; and

wherein the source region of the transistor of the first memory cell and the source region of the transistor of the third memory cell are the same region.

49. (**Currently Amended**): The memory array of claim 48 wherein:

the plurality of memory cells further includes a fourth memory cell wherein the fourth memory cell includes at least a transistor to constitute the memory cell wherein the transistor includes:

a source region having impurities to provide ~~a~~ the first conductivity type;

a drain region having impurities to provide the first conductivity type;

a body region disposed between and adjacent to the source region and the drain region wherein the body region is electrically floating and includes impurities to provide ~~a~~ the second conductivity type wherein the second conductivity type is different than the first conductivity type;

a gate spaced apart from, and capacitively coupled to, the body region; and

wherein the memory cell includes:

a first data state representative of a first charge in the body; and

a second data state representative of a second charge in the body region wherein the second charge is substantially provided by removing charge from the body region through the source region; and

wherein the drain region of the transistor of the first memory cell and the drain region of the transistor of the fourth memory cell are the same region.

50. (**Currently Amended**): The memory array of claim 47 wherein the second charge is provided in the body of the transistor of the first memory cell in response to a ~~write control signal set includes a first signal, having a~~ first positive voltage~~,~~ applied to the drain region of the transistor of the first memory cell.

51. (**Currently Amended**): The memory array of claim 50 wherein the second charge is stored in the body region of the transistor of the first memory cell in response to removing the first positive voltage from the drain region of the transistor of the first memory cell before removing ~~the~~ a second positive voltage from the gate of the transistor of the first memory cell.

52. (**Currently Amended**): The memory array of claim 51 wherein, in response to the first and second positive voltages, the first memory cell includes a forward bias current between ~~its~~ the body region and ~~its~~ the source region of the transistor of the first memory cell.

53. (**Currently Amended**): The memory array of claim 52 wherein the second charge is stored in the body region of the transistor of the first memory cell in response to removing the first positive voltage from the drain region of the transistor of the first memory cell and wherein the source regions of the transistors of the first and second memory cells are connected to a fixed voltage.

54. (**Currently Amended**): The memory array of claim 47 wherein the first charge is comprised of an accumulation of majority carriers in the body region of the transistor of the first memory cell.

55. (**Currently Amended**): The memory array of claim 54 wherein the majority carriers accumulate in a portion of the body region ~~regions~~ that is adjacent to the source region ~~regions~~ of the transistor of each memory cell of the plurality of memory cells.

56. (**Currently Amended**): The memory array of claim 47 further including a control unit, coupled to the gate and the drain region of the transistor of the first memory cell, to provide control signals to the first ~~and second~~ memory cell ~~cells~~, wherein the first memory cell, in response to ~~a~~ first write control signals ~~signal set~~, stores the first charge in the body region of the transistor of the first memory cell.

57. (**Currently Amended**): The memory array of claim 47 ~~56~~ further including a control unit, coupled to the gate and the drain region of the transistor of the first memory cell, to provide control signals to the first ~~and second~~ memory cell ~~cells~~, wherein the first

memory cell, in response to ~~a~~ second write control signals ~~signal set~~, stores the second charge in the body region of the transistor of the first memory by removing charge from the body region of the transistor of the first memory cell through its source region.

58. (**Currently Amended**): The memory array of claim 57 wherein the control unit applies positive voltages to the drain region and gate of the transistor of the first memory cell to provide the second charge in the body region of the transistor of the first memory cell.

59. (**Currently Amended**): The memory array of claim 58 wherein the control unit applies positive voltages to the drain region and gate of the transistor of the first memory cell to provide the second charge in the body region of the transistor of the first memory cell and applies a first voltage to the drain and source regions of the transistor of the second memory cell to maintain the data state of the second memory cell.

60. (**Previously Presented**): The memory array of claim 59 wherein the first voltage is ground.